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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Leonard Forbes et al.

Title: METHOD FOR OPERATING A DEAPROM HAVING AN AMORPHOUS SILICON CARBIDE GATE INSULATOR

Docket No.: 303.354US2

Serial No.: 09/135,413

Filed: August 14, 1998

Due Date: October 9, 1999

Examiner: Viet Q. Nguyen

Group Art Unit: 2818

Assistant Commissioner for Patents  
Washington, D.C. 20231

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We are transmitting herewith the following attached items (as indicated with an "X"):

- X A return postcard.
- X An Amendment and Response (7 Pages).
- X A check in the amount of \$390.00 to cover the fee for additional claims as calculated below.

If an additional fee is required due to changes to the claims, the fee has been calculated as follows:

CLAIMS AS AMENDED						
	(1) Claims Remaining After Amendment		(2) Highest Number Previously Paid For	(3) Present Extra	Rate	Fee
TOTAL CLAIMS	35	-	22	13	x 18 =	\$234.00
INDEPENDENT CLAIMS	7	-	5	2	x 78 =	\$156.00
[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED						\$0.00
TOTAL						\$390.00

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this Transmittal Letter and the paper, as described above, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on this 12<sup>th</sup> day of October, 1999.

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(GENERAL)

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AMENDMENT AND RESPONSE

Assistant Commissioner for Patents  
Washington, D.C. 20231

In response to the Office Action mailed July 9, 1999, please amend the above identified patent application as follows:

IN THE CLAIMS

Please amend the claims as follows:

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15 43. (Amended) A method for operating a floating gate transistor comprising:  
programming the floating gate transistor by inducing charge to migrate from a channel in a substrate through [a] an amorphous silicon carbide (a-SiC) gate insulator to a floating gate electrode in the floating gate transistor; and

erasing the floating gate transistor by inducing charge to migrate from the floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel.

16 44. (Amended) The method of claim 43 wherein:  
programming comprises programming the floating gate transistor by inducing hot electron injection from a channel in a substrate through [an] the amorphous silicon carbide (a-SiC) gate insulator to a polysilicon floating gate electrode in the floating gate transistor; and  
erasing comprises erasing the floating gate transistor by inducing charge to migrate from the polysilicon floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel through Fowler-Nordheim tunneling.

19 47. (Amended) A method for operating a floating gate transistor connected to a control line and a data line, the method comprising:

programming the floating gate transistor by providing a control voltage on the control